Method for Fabricating Semiconductor Memories with Charge Trapping Memory Cells

TECHNICAL FIELD

[0001] The present invention relates generally to semiconductor devices, and more particularly, the preferred embodiment relates to a method for fabricating semiconductor memories with charge trapping memory cells.

BACKGROUND

[0002] In the fabrication of electronic components, a plurality of component planes are fabricated in successive process steps. On account of the further miniaturization of these components, the problem arises that the technical means used in this case, in particular the masks, have to be oriented relative to the respective intermediate product of the component in such a way that the various planes are arranged in the envisaged manner with respect to one another.

[0003] This requirement demands a very exact alignment of the masks not only relative to the component as a whole but specifically relative to the respectively preceding arrangement of the masks, which is critical for the relative positions of the component structures. A corresponding orientation of the component planes in successive steps of the fabrication process is made more difficult due to the fact that the structures fabricated often do not produce a sufficient optical contrast and so cannot be identified accurately enough in subsequent method steps. That makes it considerably more difficult in particular to align the masks used in later fabrication steps.

SUMMARY OF THE INVENTION

[0004] The preferred embodiment of the present invention relates to a method for fabricating semiconductor memories with charge trapping memory cells in which buried bit lines are provided with bit line contacts. In various aspects, this invention solves alignment problems in the fabrication of semiconductor memories with charge trapping memory cells, in particular of NROM memory cells.

[0005] Semiconductor memories of this type have buried bit lines fabricated by doping strip-type regions of a semiconductor body. Oxide-nitride-oxide storage layer sequences are provided for the programming of the memory cells. Hot electrons from the channel are trapped in the middle layer, i.e., in the nitride layer, thereby altering the threshold voltage of the transistor cell. In order to erase the cell, the electrons are removed from the storage layer. The storage layer sequence is provided as gate dielectric between a respective channel region in the semiconductor body and a gate electrode arranged thereabove. The gate electrodes are connected to one another by strip-type word lines provided on the top side.

[0006] Bit line contacts are fabricated at regular intervals between the word lines, so that it is possible to reduce the electrical bulk resistances of the buried bit lines by conductive connections on the top side. In this case, the problem described above arises such that, in the case of the positions of the bit lines and the bit line contacts being aligned with the active regions in the manner that has been customary hitherto, manufacturing fluctuations occur which are no longer tolerable in the context of increasing miniaturization of the memory cells, since the position of the bit line contacts can no longer be set sufficiently accurately with respect to the buried bit lines.

[0007] In one aspect, the present invention specifies an improved method for aligning the bit line contacts with buried bit lines. For example, a method for manufacturing a semiconductor device includes forming a storage layer over a semiconductor body. The storage layer includes a first boundary layer (e.g., oxide), an intermediate storage layer (e.g., nitride), and a second boundary layer (e.g., oxide). The storage layer is patterned so that at least some of the storage layer is removed from over a first portion of the semiconductor body and some of the storage layer is removed from over a second portion of the semiconductor body. The first portion of the semiconductor body is doped and the second portion of the semiconductor body is etched.

[0008] By means of the method, alignment marks (alignment structures) are produced together with the bit lines as depressions in the semiconductor body or substrate. These alignment marks enable the fabrication plane of the bit line contacts to be exactly aligned directly with the position of the bit lines. The alignment marks are defined using the same mask with which the position of the buried bit lines is also defined. In this case, a particularly preferred exemplary embodiment provides for the application of an auxiliary layer, preferably made of polysilicon, nitride, nitride + oxide or other materials suitable for hard masks, which is used as a mask for etching the alignment marks. A hard mask is not absolutely necessary, however, as is shown from the explanations below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0010] Figure 1 shows the structure of the mask used, in cross section;

[0011] Figure 2 shows the intermediate product fabricated using the mask, in cross section;

[0012] Figure 3 shows the configuration of a further mask, in cross section;

[0013] Figure 4 shows a subsequent etching process, in cross section;

[0014] Figure 5 shows the structure of an alignment mark, in cross section;

[0015] Figure 6 shows the auxiliary layer and the structure of the mask, in cross section;

[0016] Figure 7 shows an intermediate product fabricated using the mask, in cross section;

[0017] Figure 8 shows the structure of the auxiliary layer and of a further mask, in cross section;

[0018] Figure 9 shows the etching process of the alignment marks in cross section; and

[0019] Figure 10 shows the structure of a finished alignment mark.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0020] The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0021] The present invention will be described with respect to preferred embodiments in a specific context, namely a semiconductor memory device that stores charge in a storage layer sequence. Aspects of the invention may also be applied, however, to other semiconductor devices that can utilize alignment markings.

[0022] The preferred embodiment will now be described with respect to Figures 1-5. For exact alignment of the fabrication plane of the bit line contacts in memories with an ONO storage layer sequence (2, 3, 4), alignment marks (12) are produced together with the bit lines (9) as depressions in the semiconductor body (1) using the same mask. As will be described with respect to Figures 6-10, a particularly preferred exemplary embodiment provides for the application of an auxiliary layer, preferably made of polysilicon, which is used as a mask for etching the alignment marks.

[0023] Figure 1 illustrates, in cross section, a detail from a semiconductor body 1, e.g., a substrate or semiconductor layer formed on a substrate, on the top side of which a storage layer sequence is grown. The storage layer sequence includes a first boundary layer 2, a storage layer 3 and a second boundary layer 4. The storage layer sequence is provided in particular for the formation of charge trapping memory cells and may be an oxide-nitride-oxide layer sequence.

[0024] A resist mask 6 is applied to the second boundary layer 4 and patterned. The mask 6 has openings 7 in the region of the buried bit lines to be fabricated. At least one further opening 8 is present at those locations at which a respective alignment mark is provided. As is indicated by the arrows depicted, the storage layer sequence is removed in the openings 7, 8 at least down to the first boundary layer 2.

[0025] Figure 2 illustrates the structure after the removal of the storage layer 3 in the openings 7 and 8. Dopant for forming the buried bit lines 9 is then introduced, which is illustrated by the dashed contour of the buried bit line in Figure 2. In this case, it is optional whether the dopant is also introduced in the region of the further openings, as depicted in Figure 2, or whether an additional covering of the further openings is used to prevent dopant from penetrating at these locations.

[0026] Figure 3 illustrates in cross section that after the formation of the buried bit lines 9, the mask 6 is removed and replaced by a further mask 10, preferably a resist mask. The further mask 10 covers the buried bit lines 9 and has openings 11 in the region of the alignment marks to be fabricated. Figure 3 reveals that this opening 11 of the further mask 10 does not have to correspond precisely to the further opening 8 of the preceding mask 6. It suffices if a sufficiently large region is left free, since the region provided for the alignment mark is defined sufficiently precisely by the preceding etching of the storage layer 3.

[0027] As shown in Figure 4, using the further mask 10, an etching attack is then effected in the openings 11 of the mask and first of all completely removes the material of the first boundary layer 2 on the top side of the semiconductor body 1. If the material of the second boundary layer 4 corresponds to the material of the first boundary layer 2, and in particular is an oxide, the material of the second boundary layer 4 is likewise completely removed in the region of the

opening 11, as is illustrated in Figure 4. Since the storage layer sequence is not intended to fulfill the storage function in the region of the alignment mark to be fabricated, this removal has no adverse consequences. The material of the semiconductor body 1 or substrate is then etched out in the region depicted in hatched fashion in the direction of the arrow depicted in Figure 4.

[0028] Figure 5 shows the structure thus achieved, in cross section, after the further mask 10 has been removed. This structure now includes an alignment mark 12 that can be used to ensure alignment of later masks. This intermediate product can then be processed further in a semiconductor memory fabrication process known per se.

[0029] In a particularly preferred further exemplary embodiment of the method, an auxiliary layer is additionally applied. Figure 6 illustrates the structure – corresponding to Figure 1 – for this further exemplary embodiment, in cross section. The storage layer sequence is applied over the whole area on the semiconductor body 1 or substrate. An auxiliary layer 5 is applied thereon, which auxiliary layer is preferably polysilicon, nitride, nitride and oxide or some other material suitable for hard masks and has a typical thickness of about 100 nm. The mask 6 is applied thereon and patterned in the manner already described, so that is has openings 7 in the region of the buried bit lines to be fabricated and at least one further opening 8 in the region of each alignment mark to be fabricated.

[0030] After the material of the auxiliary layer 5 and the material of the storage layer sequence have been etched out down to the first boundary layer 2 in the region of the openings of the mask 6, the dopant for forming the buried bit lines 9 may again be introduced, in accordance with the cross section of Figure 7. If necessary, in the opening 14 of the auxiliary layer 5 in the region of the bit lines to be fabricated, spacer elements, i.e., the spacers 15, which are depicted by dashed lines in Figure 7, may be fabricated at the sidewalls of the auxiliary layer 5. That is

done in the manner known per se by conformal whole-area deposition of the material provided for the spacers and subsequent anisotropic etching-back. The spacers 15 additionally reduce the dimension of the opening 14, so that the doped regions provided for the buried bit lines may be offset to a somewhat greater extent than the remaining portions of the storage layer sequence. A further mask 16, preferably a resist mask, is then applied, which leaves free the regions provided for the alignment marks, i.e., the openings 13 in the auxiliary layer 5.

[0031] Figure 8 illustrates this further mask 16, in cross section. It can be seen here that the openings 17 of the further mask 16, as in the preceding exemplary embodiment, do not have to have the same dimensions as the openings 13 of the auxiliary layer 5. The openings 17 in the further mask 16 may have larger dimensions; it is only necessary to leave free the region of the alignment mark to be fabricated. The opening 17 is preferably, but not necessarily, the same size or larger than the opening 13. Material of the first boundary layer 2 still present is possibly removed first of all using said further mask 16.

[0032] A cutout 18 may then be etched into the semiconductor material in the direction of the arrow in accordance with the illustration of Figure 9. If the auxiliary layer 5 is polysilicon, the polysilicon of the auxiliary layer 5 is likewise removed in the region of the opening 17 during the etching process.

[0033] Figure 10 shows the structure achieved, in cross section, after the further mask 16 and the auxiliary layer 5 have been removed. The opening 12 provided for the alignment mark in the semiconductor material may be slightly laterally expanded (etched bottle effect) if the material of the auxiliary layer 5 was polysilicon and the material of the semiconductor body or substrate is silicon and is therefore removed again during the removal of the auxiliary layer. That

does not impair the function of the alignment mark since the alignment mark has sufficiently small dimensions.

[0034] In the case of an oxide-nitride-oxide storage layer sequence, the etching processes may be performed by dry etching or wet etching using DHF or phosphoric acid, while the semiconductor material, in particular silicon, is removed by anisotropic RIE etching (reactive ion etching). The auxiliary layer is removed e.g., wet-chemically selectively with respect to the oxide of the second boundary layer 3, e.g., using NH_4OH.

[0035] While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.